(Translation)

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Application Number: Patent Application No. 10-2000-0033980

Date of Application: June 20, 2000

Applicant(s): HYNIX SEMICONDUCTOR Inc.

COMMISSIONER

[ABSTRACT]

[Summary]

The present invention relates to a method of forming a metal wiring in a semiconductor device. In order to improve a low deposition speed in the process technology by which a damascene pattern of an ultra-fine structure is filled with copper by CVD method, the present invention uses a CECVD method by which a chemical enhancer layer for increasing the deposition speed of copper is formed and the damascene pattern is then filled by means of MOCVD method using a copper precursor with forms a copper wiring, wherein the diffusion prevention film is formed on the sidewall of the damascene pattern in the shape of a spacer in order to prevent an increase of the via resistance by the diffusion prevention film in the via portion and the chemical enhancer layer is selectively formed on the etch prevention film and the lower metal layer that are exposed by the damascene pattern, thus allowing a selective partial filling. Therefore, the present invention can facilitate copper filling in an ultra-fine structure and also maximize an electrical resistivity of the copper wiring.

[Representative Drawing]

Fig. 1

[Index Word]

metal wiring, diffusion prevention film, copper precursor, CECVD method

[SPECIFICATION]

[Title of the Invention]

METHOD OF FORMING METAL WIRING IN SEMICONDUCTOR DEVICE

[Brief Description of the Drawings]

Figs. 1a to 1c are cross-sectional views for sequentially illustrating a method of forming a metal wiring in a semiconductor device according to the present invention.

<The Reference Numerals in The Drawings>

10: semiconductor substrate	20: first interlayer insulating film
30: lower metal layer	40a: first insulating film
40b: second insulating film	40c: third insulating film
40: second interlayer insulating film	50: diffusion prevention film spacer
60: chemical enhancer layer	70: copper wiring

[Detailed Description of the Invention]

[Object of the Invention]

[Technological Background of the Invention and Description of the Prior Art]

The invention relates to a method of forming a metal wiring in a semiconductor device and more particularly, to a method of forming a metal wiring in a semiconductor device by which copper can be selectively filled and an increase of the via resistance in the copper wiring due to a diffusion prevention film can be prevented,

in a process technology by which a chemical enhancer layer that can accelerate a deposition of copper is formed and a damascene pattern of an ultra-fine structure is then filled with copper using a copper precursor.

As the integration level of semiconductor devices is increased and its signal transfer speed is lowered, there has been an effort to use copper as a metal wiring for transferring current, which is lower about 40% in the resistivity than a conventional aluminum. Copper has a good electrical conductivity. However, copper has a disadvantage that the diffusion speed into a silicon oxide used as an insulating film in a semiconductor device is too fast. As copper atoms moved by diffusion of a silicon oxide degrades transistors and capacitors in the semiconductor device and thus increase the leakage current, it is necessary to use a diffusion prevention film for preventing diffusion of copper. In a dual damascene structure, however, when a copper wiring is formed, as the diffusion prevention film exists in the bottom of the via contact, it functions to increase the via resistance in the copper wiring. Therefore, if a prevention barrier metal having a low resistivity is not suitably selected, it is thought that the effect of resistance will be great and dishing and erosion may be caused by the difference of a selective ratio with the diffusion barrier film during chemical mechanical polishing (CMP) process of copper.

In addition, due to rapid higher performance and miniaturization of next-generation semiconductor device, there is a trend that a method of forming a copper wiring using CVD is applied. However, filling of copper using the CVD method has problems that the deposition speed is low and the cost is high. Recently,

there is a growing interest in filling of copper wiring using chemically enhanced chemical vapor deposition (CECVD) method. This method, however, has a problem that the chemical enhancer must be uniformly sprayed and a selective filling method must be applied by which the chemical enhancer is distributed at a specific location.

[Technical Means for Achieving the Object of the Invention]

It is therefore an object of the present invention to provide a method of forming a metal wiring in a semiconductor device capable of preventing an increase in the via resistance by forming a diffusion prevention film on the sidewall of a damascene pattern in the form of a spacer, and also facilitating a selective partial filling of the damascene pattern using a copper precursor by selectively forming a chemical enhancer layer within the damascene pattern using a selective reaction property of the chemical enhancer.

In order to accomplish the above object, a method of forming a metal wiring in a semiconductor device according to the present invention is characterized in comprising the steps of: providing a semiconductor substrate in which an interlayer insulating film including of a first, a second and a third insulating films is formed on a lower metal layer; forming a damascene pattern consisted of a trench and a via on the interlayer insulating film; forming a diffusion prevention film spacer on the sidewall of the trench and the via; selectively forming a chemical enhancer layer on the second insulating film constituting the bottom of the trench and on the lower metal layer constituting the bottom of the via; forming a copper layer by means of chemical vapor

deposition method; and performing a hydrogen reduction annealing and a chemical mechanical polishing process to form a copper metal wiring.

[Structure and Operation of the Invention]

Hereinafter, the present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings.

Figs. 1a ~ 1c are cross-sectional views for sequentially illustrating a method of forming a metal wiring in a semiconductor device according to the present invention.

Referring now to Fig. 1a, a first interlayer insulating film (20), a lower metal layer (30) and a second interlayer insulating film (40) are sequentially formed on a semiconductor substrate (10) in which various components for forming a semiconductor device is formed. The second interlayer insulating film (40) is consisted of a first insulating film (40a), a second insulating film (40b) and a third insulating film (40c). Of them, the second insulating film (40b) is made of a nitride material and serves as an etch prevention film for preventing the first insulating film (40a) from being etched upon formation of a trench is formed during the process of forming a damascene pattern in the second interlayer insulating film (40). Then, a damascene pattern consisted of the trench and via is formed in the second interlayer insulating film (40) and a cleaning process is performed to remove an oxide layer remaining on the surface of the lower metal layer (30) that is exposed by the damascene pattern. Next, a diffusion prevention film is formed in a thickness of 50 to 500 Å on the second interlayer insulating film (40) including the exposed lower metal layer (30) and is then performed a blanket etch process so that the diffusion prevention

film can be remained only at the sidewall of the damascene pattern, thus forming a diffusion prevention film spacer (50).

The first and third insulating films (40a) and (40c) are formed of oxide materials having a low dielectric constant and the second insulating film (40b) is formed of a nitride material. The trench and via formed in the second interlayer insulating film (40) is formed in a double damascene pattern. The cleaning process may employ an RF plasma in case that the lower metal layer (30) is made of a metal such as W, Al, etc., and employ a reactive cleaning method in case that the lower metal layer (30) is made of Cu. The diffusion prevention film may be formed using at least one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN, CVD WN, CVD TiAlN, CVD TiSiN and CVD TaSiN. The reason why the diffusion prevention film is formed in the shape of a spacer is that the via resistance is increased by the resistance component of the diffusion prevention film if the diffusion prevention film is formed including the surface of the lower metal layer (30).

In other words, the diffusion prevention film spacer (50) can play its role sufficiently to prevent an outward diffusion of copper atom since it covers the first and third insulating films (40a) and (40c) within the damascene pattern. In addition, the diffusion prevention film spacer (50) can lower the via resistance since the surface of the lower metal layer (30) is exposed. The diffusion prevention film spacer (50) may be formed of a nonconductor such as a silicon nitride (SiN) film or a silicon oxynitride (SiON) film since it does not exist in the bottom of the via.

Referring now to Fig. 1b, a chemical enhancer layer (60) is formed on the

entire structure including the lower metal layer (30). The chemical enhancer layer (60) has a selective reaction property which means that the chemical enhancer layer rarely reacts with an oxide material and well reacts with a nitride material and a metal. Therefore, the chemical enhancer layer (60) is not formed on the third insulating film (40c) made of an oxide material and is formed only on the second insulating film (40b) made of a nitride material and the lower metal layer (30), as shown in Fig. 1b.

The chemical enhancer layer (60) is formed in a thickness of 50 to 500Å. A catalyst for forming the chemical enhancer (60) may include one of I (iodine)-containing liquid compounds such as CH_3I, C_2H_5I, CD_3I, CH_2I_2 etc., Hhfac1/2H_2O, Hhfac, TMVS, pure I_2, I (iodine)-containing gas and water vapor, and is performed at the temperature of -20 to 300℃ for 1 to 600 seconds. Also, the catalyst may include F, Cl, Br, I, At of a liquid state and F, Cl, Br, I, At of a gas state, which are 7-group elements in the periodic table.

Referring now to Fig. 1c, a copper layer is formed on the second interlayer insulating film (40) including the damascene pattern by means of metal organic chemical vapor deposition (MOCVD) method using at least one of all the precursors of hfac series such as (hfac) CuVTMOS series, (hfac) CuDMB series, and (hfac) CuTMVS series, so that the damascene pattern is filled with copper. As the chemical enhancer layer (60) is formed on the second insulating film (40b) and the lower metal layer (30), the speed of copper being deposited into the damascene pattern is much faster than the speed of copper being deposited on the third insulating film (40c). Thus, a selective copper deposition into the damascene pattern can be made. The above selective deposition process may be performed in all the deposition equipments having

a vaporizer of direct liquid injection (DLI), control evaporation mixer (CEM), orifice scheme and spray scheme. Thereafter, a hydrogen reduction annealing process is performed and the copper layer deposited on the third insulating film (40c) is then removed by chemical mechanical polishing (CMP), thus forming a copper wiring (70). Though, the copper layer may be formed on the third insulating film 40c, it is accelerated by the chemical enhancer layer (60). Thus, as the copper layer deposited on the third insulating film (40c) is very thin in a thickness, it can be easily removed by CMP process.

In the above embodiment, it was explained that copper (Cu) is used as a material for forming a metal wiring. However, it should be noted that other metals such as aluminum or tungsten might be used instead.

[Effect of the Invention]

As mentioned above, the present invention forms a diffusion prevention film in the form of a spacer, forms a chemical enhancer layer selectively within a damascene pattern and then deposits copper to form a wiring. Therefore, the present invention has outstanding effects that it can reduce the via resistance component and thus improve the operating speed and reliability of devices.

[CLAIMS]

[Claim 1]

A method of forming a metal wiring in a semiconductor device, comprising the steps of:

providing a semiconductor substrate in which an interlayer insulating film including a first, a second and a third insulating films is formed on a lower metal layer;

forming a damascene pattern consisted of a trench and a via on said interlayer insulating film;

forming a diffusion prevention film spacer on the sidewall of said trench and via;

selectively forming a chemical enhancer layer on said second insulating film constituting the bottom of said trench and on said lower metal layer constituting the bottom of said via;

forming a copper layer by means of chemical vapor deposition method; and

performing a hydrogen reduction annealing and a chemical mechanical polishing process to form a copper metal wiring.

[Claim 2]

The method of forming a metal wiring in a semiconductor device according to claim 1, wherein a cleaning process performed after formation of said damascene pattern employs a RF plasma in case that said lower metal layer is one of W and Al, and employs a reactive cleaning process in case that said lower metal layer is Cu.

[Claim 3]

The method of forming a metal wiring in a semiconductor device according to claim 1, wherein said diffusion prevention film spacer is formed by forming a diffusion prevention film in a thickness of 50 Å to 500 Å on the entire structure including said damascene pattern and then performing a blanket etch process.

[Claim 4]

The method of forming a metal wiring in a semiconductor device according to claim 1, wherein said diffusion prevention film spacer is formed by using at least one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN, CVD WN, CVD TiAlN, CVD TiSiN and CVD TaSiN.

[Claim 5]

The method of forming a metal wiring in a semiconductor device according to claim 1, wherein said diffusion prevention film spacer is formed by using SiN or SiON.

[Claim 6]

The method of forming a metal wiring in a semiconductor device according to claim 1, wherein said chemical enhancer layer is formed in a thickness of 50 Å to 500 Å, by processing, as a catalyst, one of I (iodine)-containing liquid compound, Hhfac1/2H_2O, Hhfac, TMVS, pure I_2, I (iodine)-containing gas, water vapor, F, Cl, Br,

I, and At of a liquid state, and F, Cl, Br, I and At of a gas state, which are 7-group elements in the periodic table, at a temperature in the range of -20℃ to 300℃ for 1 to 600 seconds,

[Claim 7]

The method of forming a metal wiring in a semiconductor device according to claim 6, wherein said I (iodine)-containing liquid compound is one of CH_3I, C_2H_5I, CD_3I and CH_2I_2.

[Claim 8]

The method of forming a metal wiring in a semiconductor device according to claim 1, wherein said copper layer is formed in a deposition apparatus having a vaporizer of direct liquid injection (DLI), control evaporation mixer (CEM), orifice scheme and spray scheme by means of metal organic chemical vapor deposition (MOCVD) method, by using any one of all the precursors using hfac such as (hfac) CuVTMOS series, (hfac) CuDMB series, (hfac) CuTMVS series, and so on.

No. 9-5-2003-008484160
Date : March 06, 2003
Due Date : May 06, 2003

NOTICE OF REJECTION

Applicant :

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Agent : Young Moo Shin

Filing No. 10-2000-0033980 (Patent)

Title of the invention : Method of forming metal wiring in semiconductor device

Notice is given pursuant to Article 63 of Patent Law rejecting the above application on the ground as set forth below. If the applicant has any opinion regarding this official action, please submit such an opinion by due date.

GROUND

The subject matters in claims could easily have been made by a person with ordinary skill in the pertinent art under Article29(2) as indicated below:

Claim 1 recites a method of forming a metal wiring in a semiconductor device, comprising the steps of: forming an interlayer insulating film on a lower metal layer; forming a damascene pattern; forming a diffusion prevention film spacer; selectively forming a chemical enhancer layer on a second insulating film constituting a bottom of a trench and on a lower metal layer constituting a bottom of a via; forming a copper layer by means of a chemical vapor deposition

method; and performing a hydrogen reduction annealing and a chemical mechanical polishing process to form a copper metal wiring. However, Korean Patent Laid-Open 1998-65748(1998. 10. 15)("Cited Reference 1") relates to a method of forming a metal wiring in a semiconductor device using a damascene method by means of a chemical mechanical polishing (CMP), and discloses a method of forming a metal wiring in a semiconductor device, comprising: a first process of forming a flaw for forming a metal wiring of a semiconductor device in an insulation film; a second process of forming an intestinal wall metal film over the whole surface of the insulation film, in which the flaw is formed; a third process of forming a metal material layer on the intestinal wall metal film; a fourth process of covering the metal material layer with a viscous material to flatten the surface of the metal material layer; and performing a chemical mechanical polishing process until the insulation film is exposed, in order to remain the metal material layer only in the flaw, thereby forming a metal wiring. And Korean Patent Laid-Open 2000-22014(2000. 04. 25)("Cited Reference 2") discloses a chemical deposition method that a film is formed on a substrate by supplying a raw material at a gas state, wherein the film is formed by introducing a catalyst chemical species, said catalyst chemical species is not buried into the film which is formed during the deposition process and moves to the surface of the film to facilitate a surface deposition reaction of the raw material at a gas state. The aforementioned film is a copper metal film and said catalyst chemical species is a halogen element (iodine). Accordingly, claim 1 could easily have been made from the above cited references.

references.

March 06, 2003

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특허청
의견제출통지서

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출원번호 10-2000-0033980

발명의 명칭 반도체 소자의 금속 배선 형성 방법

이 출원에 대한 심사결과 아래와 같은 거절이유가 있어 특허법 제63조의 규정에 의하여 이를 통지하오니 의견이 있거나 보정이 필요할 경우에는 상기 제출기일까지 의견서 또는/및 보정서를 제출하여 주시기 바랍니다. (상기 제출기일에 대하여 매회 1월 단위로 연장을 신청할 수 있으며, 이 신청에 대하여 별도의 기간연장승인통지는 하지 않습니다.)

[이 유]

이 출원의 특허청구범위 제 1항에 기재된 발명은 그 출원전에 이 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 아래에 지적한 것에 의하여 용이하게 발명할 수 있는 것이므로 특허법 제29조 제2항의 규정에 의하여 특허를 받을 수 없습니다.

[아래]

청구항 제1항은 하부 금속층 상에 층간 절연막을 형성하는 단계, 다마신 패턴을 형성하는 단계, 확산 방지막 스페이서를 형성하는 단계, 트랜치 저면을 이루는 제 2 절연막 및 비아 저면을 이루는 하부 금속층 상에 선택적으로 화학적 강화제층을 형성하는 단계, 화학적 기상 증착법으로 구리층을 형성하는 단계, 수소 환원 열처리 및 화학적 기계적 연마공정을 실시하여 구리 금속 배선을 형성하는 단계를 포함하여 이루어지는 것을 특징으로 하는 반도체 소자의 금속 배선 형성 방법에 관한 것이지만, 한국공개특허공보제98-65748호(1998.10.15공개,인용예1)에는 반도체 소자의 금속 배선 형성에 있어서 화학 물리적 폴리싱(CMP)을 이용한 다마신 기법에 관한 것으로 절연막에 금속배선 형성을 위한 홈을 형성하는 제1 공정, 홈이 형성되어 있는 절연막 전면에 장벽금속막을 형성하는 제2 공정, 장벽금속막 상에 금속물질층을 형성하는 제3 공정, 금속물질층 상에 점성을 갖는 물질을 그 표면이 평탄하도록 도포하는 제4 공정, 절연막이 노출될 때 까지 화학 물리적 폴리싱을 행하여 홈에만 금속물질층을 남김으로써 금속 배선을 형성하는 제5 공정을 구비하는 것을 특징으로 하는 반도체 소자의 금속 배선 형성방법이 기재되어 있으며, 한국공개특허공보제2000-22014호(2000.4.25공개,인용예2)에는 기체 상태의 원료를 공급하여 기판 상에 막을 형성하는 화학 증착방법에 있어서, 증착과정 중 형성되는 막에 매몰되지 않고 그 막의 표면으로 이동하여 상기 기체 원료의 표면 증착반응을 촉진하는 촉매 화학종을 도입하여 막을 형성하는 것을 특징으로 하는 화학 증착방법이 기재되어 있으며, 상기 막이 금속 구리 막이며, 상기 촉매 화학종이 할로겐 원소(아이오딘)이라고 기재되어 있으므로 청구항 제1항은 인용예1,2에 의하여 용이발명이 가능한 것으로 판단됩니다.

[첨 부]

첨부 1 한국공개특허공보제98-65748호(1998.10.15공개,인용예1)
첨부2 한국공개특허공보제2000-22014호(2000.4.25공개,인용예2) 끝.

출력 일자: 2003/3/7

2003.03.06

특허청 심사4국

반도체1심사담당관실 심사관 김종찬

<<안내>>

문의사항이 있으시면 ☎ 042-481-5722 로 문의하시기 바랍니다.

특허청 직원 모두는 깨끗한 특허행정의 구현을 위하여 최선을 다하고 있습니다. 만일 업무처리과정에서 직원의 부조리행위가 있으면 신고하여 주시기 바랍니다.

▶ 홈페이지(www.kipo.go.kr)내 부조리신고센터

Soviet Union	1397205-15	1397205	The numbers following the slash denote the examination division and a processing division.
United States [US]	889877	889877	The highest number assigned in the series of numbers started in January 1960. New series started in January 1970, January 1979, D January 1987, January 1993, and January 1998.

ICIREPAT Country Code is indicated in brackets, e.g., [AR].

D In order to distinguish utility model applications from patent applications, it is necessary to identify them as to type of application in citations or references. This may be done by using the name of the application type in conjunction with the number or by using the symbol "U" in brackets or other enclosure following the number.

201.15 Right of Priority, Overcoming a Reference

The only times during *ex parte* prosecution that the examiner considers the merits of an applicant's claim of priority is when a reference is found with an effective date between the date of the foreign filing and the date of filing in the United States and when an interference situation is under consideration. If at the time of making an action the examiner has found such an intervening reference, he or she simply rejects whatever claims may be considered unpatentable thereover, without paying any attention to the priority date (assuming the papers have not yet been filed). The applicant in his or her reply may argue the rejection if it is of such a nature that it can be argued, or present the foreign papers for the purpose of overcoming the date of the reference. If the applicant argues the reference, the examiner, in the next action in the application, may specifically require the foreign papers to be filed in addition to repeating the rejection if it is still considered applicable, or he or she may merely continue the rejection.

Form paragraph 2.19 may be used in this instance.

✓ ¶ *2.19 Overcome Rejection by Translation*

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Examiner Note

This paragraph should follow a rejection based on an intervening reference.

In those cases where the applicant files the foreign papers for the purpose of overcoming the effective date of a reference, a translation is required if the foreign papers are not in the English language. When the examiner requires the filing of the papers, the translation should also be required at the same time. This translation must be filed together with a statement that the translation of the certified copy is accurate. When the necessary papers are filed to overcome the date of the reference, the examiner's action, if he or she determines that the applicant is not entitled to the priority date, is to repeat the rejection on the reference, stating the reasons why the applicant is not considered entitled to the date. If it is determined that the applicant is entitled to the date, the rejection is withdrawn in view of the priority date.

If the priority papers are already in the file when the examiner finds a reference with the intervening effective date, the examiner will study the papers, if they are in the English language, to determine if the applicant is entitled to their date. If the applicant is found to be entitled to the date, the reference is simply not used but may be cited to applicant on form PTO-892. If the applicant is found not entitled to the date, the unpatentable claims are rejected on the reference with an explanation. If the papers are not in the English language and there is no translation, the examiner may reject the unpatentable claims and at the same time require an English translation for the purpose of determining the

applicant's right to rely on the foreign filing date.

The foreign application may have been filed by and in the name of the assignee or legal representative or agent of the inventor, as applicant. In such cases, if the certified copy of the foreign application corresponds with the one identified in the oath or declaration as required by 37 CFR 1.63 and no discrepancies appear, it may be assumed that the inventors are entitled to the claim for priority. If there is disagreement as to inventors on the certified copy, the priority date should be refused until the inconsistency or disagreement is resolved.

The most important aspect of the examiner's action pertaining to a right of priority is the determination of the identity of invention between the U.S. and the foreign applications. The foreign application may be considered in the same manner as if it had been filed in this country on the same date that it was filed in the foreign country, and the applicant is ordinarily entitled to any claims based on such foreign application that he or she would be entitled to under our laws and practice. The foreign application must be examined for the question of sufficiency of the disclosure under 35 U.S.C. 112, as well as to determine if there is a basis for the claims sought.

In applications filed from the United Kingdom there may be submitted a certified copy of the "provisional specification," which may also in some cases be accompanied by a copy of the "complete specification." The nature and function of the United Kingdom provisional specification is described in an article in the Journal of the Patent Office Society of November 1936, pages 770-774. According to United Kingdom law the provisional specification need not contain a complete disclosure of the invention in the sense of 35 U.S.C. 112, but need only describe the general nature of the invention, and neither claims nor drawings are required. Consequently, in considering such provisional specifications, the question of completeness of disclosure is important. If it is found that the United Kingdom provisional specification is insufficient for lack of disclosure, reliance may then be had on the complete specification and its date, if one has been presented, the complete specification then being treated as a different application and disregarded as to the requirement to file within 1 year.
In some instances, the specification and drawing of the foreign application may have been filed at a date subsequent to the filing of the petition in the foreign country. Even though the petition is called the application and the filing date of this petition is the filing date of the application in a particular country, the date accorded here is the date on which the specification and drawing were filed.

It may occasionally happen that the U.S. application will be found entitled to the filing date of the foreign application with respect to some claims and not with respect to others. Occasionally a sole or joint applicant may rely on two or more different foreign applications and may be entitled to the filing date of one of them with respect to certain claims and to another with respect to other claims.

abandonment by the parties thereof...". It is therefore clear that an international application which designates the United States has the effect of a pending U.S. application from the international application filing date until its abandonment as to the United States. The first sentence of 35 U.S.C. 365(c) specifically provides that "In accordance with the conditions and requirements of section 120 of this title,... a national application shall be entitled to the benefit of the filing date of a prior international application designating the United States." The condition of 35 U.S.C. 120 relating to the time of filing requires the later application to be "filed before the patenting or abandonment of or termination of proceedings on the first application...". The filing of a continuation or continuation-in-part application of an international application may be useful to patent applicants where the oath or declaration required by 35 U.S.C. 371(c)(4) cannot be filed as required by 37 CFR ** 1.495. An applicant filing an application under 35 U.S.C. 111(a) and 37 CFR 1.53(b) may obtain additional time to file the oath or declaration under 37 CFR 1.53(f) and 1.136(a).

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201.12 Assignment Carries Title

Assignment of an original application carries title to any divisional, continuation, or reissue application stemming from the original application and filed after the date of assignment. See MPEP § 306. When the assignment is in a provisional application, see MPEP § 306.01.

201.13 [R-1] Right of Priority of Foreign Application

Under certain conditions and on fulfilling certain requirements, an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country, to overcome an intervening reference or for similar purposes. The conditions are specified in 35 U.S.C. 119(a)-(d) and (f).

35 U.S.C. 119. Benefit of earlier filing date; right of priority.

(a) An application for patent for an invention filed in this country by any person who has, or whose legal representatives or assigns have, previously regularly filed an application for a patent for the same invention in a foreign country which affords similar privileges in the case of applications filed in the United States or to citizens of the United States, or in a WTO member country, shall have the same effect as the same application would have if filed in this country on the date on which the application for patent for the same invention was first filed in such foreign country, if the application in this country is filed within twelve months from the earliest date on which such foreign application was filed; but no patent shall be granted on any application for patent for an invention which had been patented or described in a printed publication in any country more than one year before the date of the actual filing of the application in this country, or which had been in public use or on sale in this country more than one year prior to such filing.

(b)

(1) No application for patent shall be entitled to this right of priority unless a claim is filed in the Patent and Trademark Office, identifying the foreign application by specifying the application number on that foreign application, the intellectual property authority or country in or for which the application was filed, and the date of filing the application, at such time during the pendency of the application as required by the Director.

(2) The Director may consider the failure of the applicant to file a timely claim for priority as a waiver of any such claim. The Director may establish procedures, including the payment of a surcharge, to accept an unintentionally delayed claim under this section.

(3) The Director may require a certified copy of the original foreign application, specification, and drawings upon which it is based, a translation if not in the English language, and such other information as the Director considers necessary. Any such certification shall be made by the foreign intellectual property authority in which the foreign application was filed and show the date of the application and of the filing of the specification and other papers.

(c) In like manner and subject to the same conditions and requirements, the right provided in this section may be based upon a subsequent regularly filed application in the same foreign country instead of the first filed foreign application, provided that any foreign application filed prior to such subsequent application has been withdrawn, abandoned, or otherwise disposed of, without having been laid open to public inspection and without leaving any rights outstanding, and has not served, nor thereafter shall serve, as a basis for claiming a right of priority.

(d) Applications for inventors ' certificates filed in a foreign country in which applicants have a right to apply, at their discretion, either for a patent or for an inventor 's certificate shall be treated in

this country in the same manner and have the same effect for purpose of the right of priority under this section as applications for patents, subject to the same conditions and requirements of this section as apply to applications for patents, provided such applicants are entitled to the benefits of the Stockholm Revision of the Paris Convention at the time of such filing.

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37 CFR 1.55. Claim for foreign priority.

(a) An applicant in a nonprovisional application may claim the benefit of the filing date of one or more prior foreign applications under the conditions specified in 35 U.S.C. 119(a) through (d) and (f), 172, and 365(a) and (b).

(1)

(i) **> In an original application filed under 35 U.S.C. 111(a), the claim for priority must be presented during the pendency of the application, and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. This time period is not extendable. The claim must identify the foreign application for which priority is claimed, as well as any foreign application for the same subject matter and having a filing date before that of the application for which priority is claimed, by specifying the application number, country (or intellectual property authority), day, month, and year of its filing. The time periods in this paragraph do not apply in an application under 35 U.S.C. 111(a) if the application is:

(A) A design application; or

(B) An application filed before November 29, 2000.<

(ii) In an application that entered the national stage from an international application after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and the Regulations under the PCT.

(2) The claim for priority and the certified copy of the foreign application specified in 35 U.S.C. 119(b) or PCT Rule 17 must, in any event, be filed before the patent is granted. If the claim for priority or the certified copy of the foreign application is filed after the date the issue fee is paid, it must be accompanied by the processing fee set forth in § 1.17(i), but the patent will not include the priority claim unless corrected by a certificate of correction under 35 U.S.C. 255 and § 1.323

(3) When the application becomes involved in an interference (§ 1.630), when necessary to overcome the date of a reference relied upon by the examiner, or when deemed necessary by the examiner, the Office may require that the claim for priority and the certified copy of the foreign application be filed earlier than provided in paragraphs (a)(1) or (a)(2) of this section.

(4) An English language translation of a non-English language foreign application is not required except when the application is involved in an interference (§ 1.630), when necessary to overcome the date of a reference relied upon by the examiner, or when specifically required by the examiner. If an English language translation is required, it must be filed together with a statement that the translation of the certified copy is accurate.

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